MT6357 PMIC Technical Brief

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Document Revision History

Revision	Date	Author	Description
0.1	2017-03-29	Zax Lo	Initial draft

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.6V ~ 5V
- 5 buck converters and 29 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- SPI interface
- USB Battery Charging Specification ver BC1.2 Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 209-pin VFBGA package

1.2 Applications

MT6357 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6357 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 5 buck converters and 29 LDOs optimized for specific 2G/3G/4G smart phone subsystems.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6357 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6357 adopts SPI interface and 2 SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6357 is available in a 209-pin VFBGA package. The operating temperature ranges from -30 to +85°C.

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1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6357V/A		-30 ~ +85°C	VFBGA 209L

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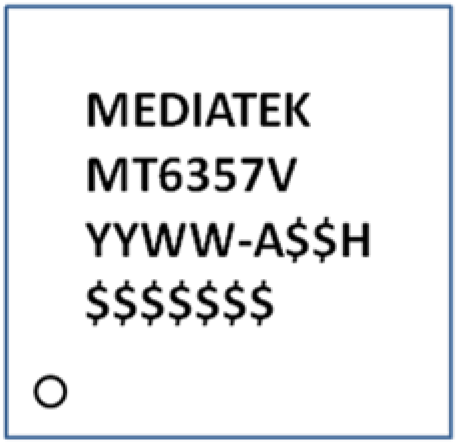
1.5 Top Marking Definition

MT6357V/A



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1.6 Pin Assignments and Descriptions

209	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VPA	VSYS_VPA	VSYS_VPA	VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	VCORE	VCORE		GND_VMODEM	VSYS_VMODEM	VSYS_VS1	GND_VS1	VS1	VCAMIO	A
B	GND_SMPS	VSYS_SMPS	GND_VPA	VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	GND_VCORE	VCORE	VMODEM	GND_VMODEM	VSYS_VMODEM	VSYS_VS1	GND_VS1	VS1	VIO18	B
C		VPROC_FB		VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	GND_VCORE	VCORE	VMODEM	GND_VMODEM					VS1_LDO1	C
D	AU_V18N	GND_VPROC_FB	VCORE_FB			D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	GND_VMODEM_FB		VRF18		D
E		FLYN	GND_VCORE_FB	VPA_FB		D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	VMODEM_FB	VS1_FB	VCN18	VRF12	VCAMD	E
F	FLYP	AVSS18_AUD	AU_LOLN	AU_LOLP	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND		VS2_LDO1		VS2_LDO2	F
G		AVDD18_AUD	AU_HPR		AU_HSN	AU_HSP	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND		VSYS_LDO1	VSRAM_PROC	VSRAM_OTHERS		G
H			AU_REFN		AVSS28_AUD	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND			VEFUSE	VCAMA	VDRAM	H
J	HP_EINT	AU_HPL		AU_VIN2_P	AU_VIN2_N	D_GND	D_GND	D_GND	D_GND	DVSS18_IO	D_GND			VUSB			VSIM1	J
K	AVDD28_AUD		AU_VIN0_P	AU_VIN0_N	AU_VIN1_P		VSYS_LDO3			DVDD18_IO		D_GND	VCN28		VIO28	VSIM2		K
L			AU_MICBIAS0		AU_VIN1_N		VAUD28			DVDD18_DIG		ISINK1		VFE28	VMC	VLDO28	VEMC	L
M	XTAL1	AVSS22_XO	AU_MICBIAS1	ACCDET	EXT_PMIC_EN1	EXT_PMIC_PG	SPI_MOSI	SPI_CLK	SPI_MISO	CHG_DM	CHG_DP		BATSNS	AUD_SYNC_MOSI		VIBR		M
N	XTAL2	AVSS22_XO_ISO	UVLO_VTH	FCHR_ENB	EXT_PMIC_EN2		SRCLKEN_IN0	SRCLKEN_IN1	VSYSSNS			PCHR_LED	ISENSE	AUD_DAT_MOSI1		VMCH	VSYS_LDO2	N
P	AVSS22_XOBUF	AVSS22_XO_ISO	XO_WCN		PMU_TESTMODE		AVSS18_AUXADC		FSOURCE		RTC32K_2V8		VDRV	RTC32K_1V8_0	AUD_DAT_MOSI0	AUD_CLK_MOSI	VCN33	P
R	AVSS22_XOBUF	XO_NFC	XO_SOC	PWRKEY	RESETB		AVDD18_AUXADC	SPI_CSN	TREF	CS_N	CHRLDO	VRTC28	BATON		RTC32K_1V8_1	AUD_CLK_MISO	AUD_DAT_MISO1	R
T	XO_CEL	XO_EXT		VXO22	VAUX18		AUXADC_VIN	WDTRST_B_IN		CS_P	VCDT		GND_VREF	VREF		AUD_SYNC_MISO	AUD_DAT_MISO0	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 1-1. MT6357 VFBGA 209 (7.0x6.6mm) pin assignment (top view)

Table 1-1. MT6357 pin descriptions

Ball	Symbol	I/O	Description
A4, B4, C4	VSYS_VPROC	PWR	Power supply of VPROC
A6, A7, B6, B7, C6, C7	VPROC	O	SW node of VPROC
A5, B5, C5	GND_VPROC	GND	VPROC ground
C2	VPROC_FB	I	BUCK VPROC feedback pin
D2	GND_VPROC_FB	I	Remote sense on ground of VPROC
A8, B8, C8	VSYS_VCORE	PWR	Power supply of VCORE
A9, A10, B10, C10	VCORE	O	SW node of VCORE
B9, C9	GND_VCORE	GND	VCORE ground
D3	VCORE_FB	I	BUCK VCORE feedback pin
E3	GND_VCORE_FB	I	Remote sense on ground of VCORE

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Ball	Symbol	I/O	Description
A13, B13	VSYS_VMODEM	PWR	Power supply of VMODEM
B11, C11	VMODEM	O	SW node of VMODEM
A12, B12, C12	GND_VMODEM	GND	VMODEM ground
E13	VMODEM_FB	I	BUCK VMODEM feedback pin on Vout
D14	GND_VMODEM_FB	I	Remote sense on ground of VMODEM Vout
A14, B14	VSYS_VS1	PWR	Power supply of VS1
A16, B16	VS1	O	SW node of VS1
A15, B15	GND_VS1	GND	VS1 ground
E14	VS1_FB	I	BUCK VS1 feedback pin
A2, A3	VSYS_VPA	PWR	Power supply of VPA
A1	VPA	O	SW node of VPA
B3	GND_VPA	GND	VPA ground
E4	VPA_FB	I	BUCK VPA feedback pin on Vout
B2	VSYS_SMPS	PWR	Power supply of buck controller
B1	GND_SMPS	GND	GND of buck controller
L14	VFE28	O	VFE28 output voltage
K13	VCN28	O	VCN28 output voltage
H16	VCAMA	O	VCAMA output voltage
R9	TREF	O	TREF output voltage
T4	VXO22	O	VXO22 output voltage
L7	VAUD28	O	VAUD28 output voltage
T5	VAUX18	O	VAUX18 output voltage
P17	VCN33	O	VCN33 output voltage
J17	VSIM1	O	VSIM1 output voltage
K16	VSIM2	O	VSIM2 output voltage
L16	VLDO28	O	VLDO28 output voltage
K15	VIO28	O	VIO28 output voltage
L15	VMC	O	VMC output voltage
N16	VMCH	O	VMCH output voltage
L17	VEMC	O	VEMC33 output voltage
M16	VIBR	O	VIBR output voltage
J14	VUSB	O	VUSB output voltage
A17	VCAMIO	O	VCAMIO output voltage
E15	VCN18	O	VCN18 output voltage
D16	VRF18	O	VRF18 output voltage
B17	VIO18	O	VIO18 output voltage
H15	VEFUSE	O	VEFUSE output voltage
E17	VCAMD	O	VCAMD output voltage
E16	VRF12	O	VRF12 output voltage
G15	VSRAM_PROC	O	VSRAM_PROC output voltage
G16	VSRAM_OTHERS	O	VSRAM_OTHERS output voltage
H17	VDRAM	O	VDRAM output voltage
C17	VS1_LDO1	PWR	2V power supply of SLDO1
F15	VS2_LDO1	PWR	Power supply of SLDO1
F17	VS2_LDO2	PWR	Power supply of SLDO2
G14	VSYS_LDO1	PWR	Power supply input of LDO group1
N17	VSYS_LDO2	PWR	Power supply input of LDO group2
K7	VSYS_LDO3	PWR	Power supply input of LDO group3
N4	FCHR_ENB	I	Forces charging disable pin (merged with HOMEKEY, same as MT6351)
N13	ISENSE	I	Positive terminal for battery's charging current sensing resistor

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Ball	Symbol	I/O	Description
M13	BATSNS	I	Negative terminal for battery's charging current sensing resistor
N9	VSYSSNS	I	VSYS supply input for internal block and UVLO detection
R13	BATON	I	Battery NTC pin for battery and its temperature sensing
T11	VCDT	I	Fractional charger input voltage for charger detection
P13	VDRV	O	Charger current drive output
R11	CHRLDO	O	CHRLDO output voltage
M10	CHG_DM	I	USB D- for BC1.2 standard
M11	CHG_DP	I	USB D+ for BC1.2 standard
N12	PCHR_LED	I	Pre-charge indicator
N3	UVLO_VTH	I	UVLO threshold control pin
T14	VREF	O	Bandgap reference voltage
T13	GND_VREF	GND	Ground for bandgap
P11	RTC32K_2V8	O	VRTC domain 32kHz clock output
R12	VRTC28	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
R4	PWRKEY	I	PWRKEY button
R5	RESETB	O	System reset release signal
P5	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
M5	EXT_PMIC_EN1	O	Ext chip enable pin1
N5	EXT_PMIC_EN2	O	Ext chip enable pin2
M6	EXT_PMIC_PG	I	Ext chip enable PGOOD detect
R10	CS_N	I	Fuel gauge ADC input pin
T10	CS_P	I	Fuel gauge ADC input pin
R7	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
P7	AVSS18_AUXADC	GND	AUXADC ground
T7	AUXADC_VIN	I	AUXADC input
P16	AUD_CLK_MOSI	I	Audio control interface
P15	AUD_DAT_MOSI0	I/O	Audio control interface
N14	AUD_DAT_MOSI1	I/O	Audio control interface
M14	AUD_SYNC_MOSI	I/O	Audio control interface
R16	AUD_CLK_MISO	O	Audio control interface
T17	AUD_DAT_MISO0	I/O	Audio control interface
R17	AUD_DAT_MISO1	I/O	Audio control interface
T16	AUD_SYNC_MISO	I/O	Audio control interface
M8	SPI_CLK	I	SPI control interface
R8	SPI_CSN	I/O	SPI control interface
M9	SPI_MISO	I/O	SPI control interface
M7	SPI_MOSI	I/O	SPI control interface
T8	WDTRSTB_IN	I	Watchdog reset from AP
N7	SRCLKEN_IN0	I	Source clock enable pin 0
N8	SRCLKEN_IN1	I	Source clock enable pin 1
L10	DVDD18_DIG	PWR	VDIG18 output voltage
K10	DVDD18_IO	PWR	Digital IO power
J10	DVSS18_IO	GND	Digital IO power GND
P14	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
R15	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
P9	FSOURCE	PWR	EFUSE power source
G3	AU_HPR	O	Earphone right channel output

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Ball	Symbol	I/O	Description
J2	AU_HPL	O	Earphone left channel output
H3	AU_REFN	GND	Audio reference ground
G5	AU_HSN	O	Handset negative output
G6	AU_HSP	O	Handset positive output
F4	AU_LOLP	O	Lineout positive output
F3	AU_LOLN	O	Lineout negative output
M4	ACCDET	I	Accessory detection input
L3	AU_MICBIAS0	O	Microphone Bias 0
M3	AU_MICBIAS1	O	Microphone Bias 1
K3	AU_VIN0_P	I	Microphone channel 0 positive input
K4	AU_VIN0_N	I	Microphone channel 0 negative input
K5	AU_VIN1_P	I	Microphone channel 1 positive input
L5	AU_VIN1_N	I	Microphone channel 1 negative input
J4	AU_VIN2_P	I	Microphone channel 2 positive input
J5	AU_VIN2_N	I	Microphone channel 2 negative input
J1	HP_EINT	I	HPL detection
G2	AVDD18_AUD	PWR	1.8V power supply of audio
F2	AVSS18_AUD	GND	Audio DL ground
F1	FLYP	O	Flying capacitor top
E2	FLYN	O	Flying capacitor bottom
D1	AU_V18N	PWR	Audio -1.8V supply
K1	AVDD28_AUD	PWR	Power supply of Audio UL
H5	AVSS28_AUD	GND	Audio UL ground
L12	ISINK1	I	ISINK channel 1
P1, R1	AVSS22_XOBUF	GND	Ground for XO
P3	XO_WCN	O	26MHz output to Conn. RF
T1	XO_CEL	O	26MHz output to Cell. RF
R2	XO_NFC	O	26MHz output to NFC
R3	XO_SOC	O	26MHz output to SOC
T2	XO_EXT	O	26MHz output to UFS
M2	AVSS22_XO	GND	Ground for XO
M1	XTAL1	I/O	XTAL input 1
N1	XTAL2	I/O	XTAL input 2
N2, P2	AVSS22_XO_ISO	GND	Connect to GSUB for DCXO noise isolation
D6, D7, D8, D9, D10, D11, D12, D13, E6, E7, E8, E9, E10, E11, E12, F5, F6, F7, F8, F9, F10, F11, F12, F13, G7, G8, G9, G10, G11, G12, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J11, K12	D_GND	GND	Ground

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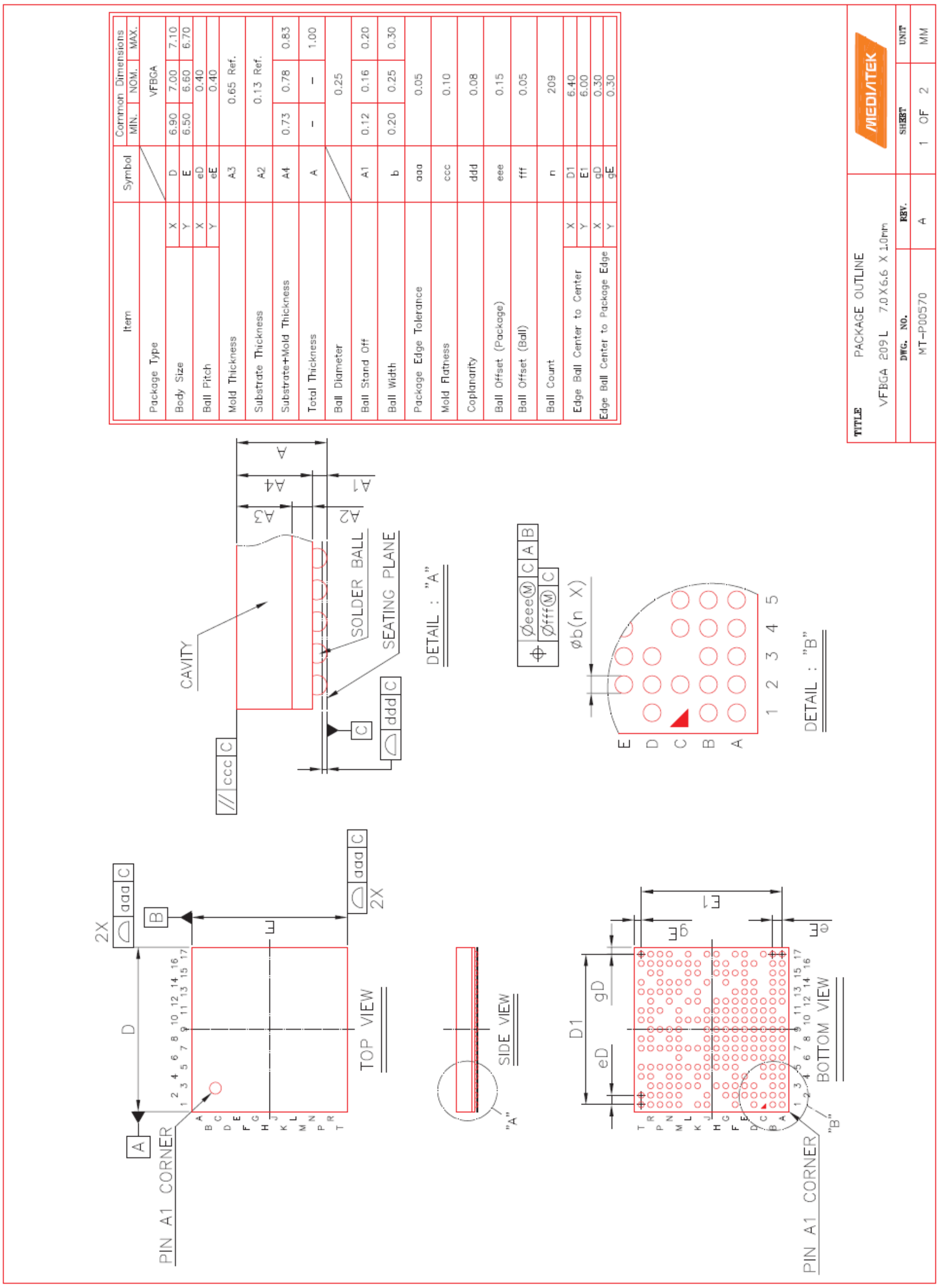
2 MT6357 Packaging

2.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	6.90	7.00	7.10
	Y	E	6.50	6.60	6.70
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.13 Ref.	
Substrate+Mold Thickness		A4	0.73	0.78	0.83
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		209	
Edge Ball Center to Center	X	D1		6.40	
	Y	E1		6.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 2-1. Package dimension

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Appendix

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